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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,676	12/22/2000	David E. Miner	42390P10141	1649

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EXAMINER	
CHUNG, PHUNG M	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,676	MINER ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005 and 18 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-22 and 24-37* is/are rejected.

7)☒ Claim(s) *7 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 37, line 2,"said at least two processor cores" does not have a clear antecedent basis.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> > (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 30-36 are rejected under 35 U.S.C. 102 (e) as being anticipated by Haroun et al (6,711,707).

As per claim 1, Haroun et al disclose an apparatus, comprising:

a multi-core processor (Fig. 1, block 3);

at least one test control mechanism (Fig. 1, block 9), including at least one test access port controller (TAPC) (Fig. 1, block 5) and a plurality of distributed data (Fig. 3(a-b), data registers) and control registers (Fig. 3a , instruction registers);

the multi-core processor and the test control mechanism having a configuration so as to allow testing of the multi-core processor (Fig. 1, blocks 1 and 11).

As per claim 30, Haroun et al disclose a method, comprising the steps of:

providing an indicator to identify a desired testing portion (col. 4, second paragraph);

based upon the desired testing portion, dynamically routing signals between a plurality test access ports (TAPs) (col. 4, line 38, dynamic connection means);

wherein the plurality test access ports (TAPs) (Fig. 1, blocks 5) are part of a multi-core processor;

the multi-processor core including a plurality of processor cores (blocks 3).

As per claim 31, Haroun et al further disclose wherein the rounting of the signals is selected from a group consisting essentially of coupling the test access ports substantially in series (col. 2, lines 52 and 60), coupling the test access ports substantially in parallel (col. 2, line 50 for connection means), and coupling the test access ports for substantially independent operation.

As per claims 32-33, Haroun et al further disclose storing control information in a register (col. 4, line 19).

As per claim 34, Haroun et al further disclose that wherein storing control informtion in a register comprise a step in compliance with the opertion of test data registers as described in the IEEE 1149.1 specification (col. 7, lines 47-60).

As per claims 35-36, Haroun et al further disclose wherein dynamically routing signals between a plurality of test access ports(TAPs) comprises dynamically routing signals between a plurality of test access port controllers (TAPCs) (Fig. 1, blocks 5) and a plurality of distributed data (Fig. 3 a-b, data registers) and control registers (Fig. 3a, instruction registers).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 2-6, 8-15, 17-22 and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haroun et al (6,711,707) in view of Champlin (5,644,580).

As per claims 2, 10-11, 13-15 and 17, Haroun et al further disclose the multi-core processor comprises at least two processor cores (Fig. 1, blocks 3). Haroun et al do not disclose wherein the multi-core processor comprises at least one circuit comprising non-processor core logic. However, Champlin discloses at least one circuit comprising non-processor core logic (Fig. 2, block 34). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate at least one circuit comprising non-processor core logic as taught by Champlin into the invention of Haroun et al so that it can be operable in a plurility of states, including an Update-DR state and a Shift-DR state, and a Boundary-Scan cell coupled between the core logic and the output pin. Isolating the output pin from the core logic during the Update-DR state when the instruction register contains an external test (EXTEST) instruction. The output pin is coupled to the core logic during the Shift-DR state when the instructiion register contains the EXTEST instruction.

As per claims 3-4 and 8-9, Haroun et al further disclose wherein the multi-core processor and the test control mechanism having a configuration so as to allow testing of at least two processor cores of the multi-core processor (Fig. 1, blocks 1 and 11).

As per claim 5, Haroun et al further disclose, wherein the at least one test control mechanism is substantially compliant with the IEEE 1149.1 specification (col. 1, lines 20-23).

As per claim 6, Haroun et al further disclose wherein the at least one test access port controller is located within the at least two processor cores (fig. 1, block 5).

As per claim 12, Haroun et al further disclose wherein the multiple coupling arrangement are selected from a group consisting essentially of coupling the test access ports substantially in series, coupling the test access porsts sybstantially in parallel and coupling the test access ports for substantially independent operation (col. 2, lines 49-62).

As per claim 18, this claim is rejected under similar rationale as set forth in claims 1-2.

As per claim 19, this claim is rejected under similar rationale as set forth in claim 3.

As per claims 20 and 24-25, thess claims are rejected under similar rationale as set forth in claims 4 and 8-9.

As per claim 21, this claim is rejected under similar rationale as set forth in claim 5.

As per claim 22, this claim is rejected under similar rationale as set forth in claim 6.

As per claims 26-27 and 29, these claims are rejected under similar rationale as set forth in claims 10-11, 13-15 and 17.

As per claim 28, this claim is rejected under similar rationale as set forth in claim 12.

6. Claims 16 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haroun et al (6,711,707) in view of Champlin (5,644,580) as applied to claims 1-2 and 30 above, and further in view of Beardsley et al (2002/0138695).

As per claim 16, the teaching of Haroun et al and Champlin have been discussed above. They do not specifically disclose wherein the at least one test control mechanism is coupled to produce during operation an error signal if the output signals of the at least two processor cores's the one test access port are not substantially equivalent. However, Beardsley et al disclose at

least one test control mechanism is coupled to produce during operation an error signal if the output signals of the at least two processor cores's the one test access port are not substantially equivalent (col. 14, lines 35-39). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the at least one test control mechanism is coupled to produce during operation an error signal if the output signals of the at least two processor cores's the one test access port are not substantially equivalent as taught by Beardsley et al into the invention of Haroun et al and Champlin to output error signals.

As per claim 37, this claim is rejected under similar rationale as set forth in claim 16.

7. Claims 7 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Applicant's arguments with respect to claims 1-37 have been considered but are moot in view of the new ground(s) of rejection.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571- 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner